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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,661	10/02/2003	Joel Howard Schopp	AUS920030739US1	9970

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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,661	SCHOPP, JOEL HOWARD	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 2 October 2003 has been fully considered by the examiner.

Drawings

2. The drawings were received on 2 October 2003. These drawings are deemed acceptable for examination.

Specification

3. The abstract of the disclosure is objected to because of the following.

All extraneous markings (such as "Docket No. ...") should be removed from the abstract.

Correction is required. See MPEP § 608.01(b).

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

5. Claims 2-3, 8, 11-12 and 18-19 are objected to because of the following informalities:

As for claim 2, Examiner recommends the phrase "is preformed" be removed (as recited on line three of this claim) for clarity. Similar objections apply to claims 11 and 18.

As for claim 8, Examiner recommends the phrase "repeating the generating set" as recited on lines 15-16 of this claim be changed to "repeating the generating a set step" for clarity.

Claims 3, 12 and 19 are further objected to for depending upon a previously objected to claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the processors" in line 15. There is insufficient antecedent basis for this limitation in the claim. It is unclear if "the processors" is referring to the unallocated processors as recited on line 14, or the removed processors as recited on line 13 of the claim. The latter is assumed, and the claim will be further treated on its merits based on this assumption.

Claim 7 recites the limitation "the processors" on line 1 and 4 of this claim. There is insufficient antecedent basis for this limitation in the claim. It is unclear if "the processors" is referring to the unallocated processors as recited on line 14 of claim 1, or the processors as recited within the preamble of claim 1. The latter is assumed, and the claim will be further treated on its merits based on this assumption.

Claim 8 recites the limitation "the set of partitions" on line 1 this claim. There is insufficient antecedent basis for this limitation in the claim. More specifically, a "set of partitions" is not previously set forth within the claim. The claim will be further treated on its merits based on this assumption that Applicant intended this limitation to read "*a* set of partitions".

Claim 9 recites the limitation "the processors" in line 19. There is insufficient antecedent basis for this limitation in the claim for the same reasons as discussed with claim 1. The examiner will make the same assumption for claim 9 as discussed with respect to claim 1.

Claims 10 and 17 recite the limitation "the processors" in line 15. There is insufficient antecedent basis for this limitation in the claim for the same reasons as discussed with claim 1. The examiner will make the same assumption for claims 10 and 17 as discussed with respect to claim 1.

The remaining pending claims are rejected for further limiting one of the previously rejected base claims.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 17-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, the "computer readable medium" as recited in these claims contains both statutory (recordable-type media – i.e. a hard disk drive), and non-statutory (transmission-type media – i.e. signals) subject matter. Descriptions for these media are presented on page 24, lines 1-19 of Applicant's specification.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 4, 8, 10 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig et al., hereinafter Olarig (US PG Publication 2003/0065886 A1).

As for claims 1, 8 and 10, Olarig teaches a method (and system) for assigning processors to partitions in a multi-processor data processing system, the method comprising:

generating optimal allocation sets for unallocated processors in the multi-processor data processing system for a cache level, wherein each set includes an allocation of unallocated processors to at least one partition (the cache can be partitioned variety of different manners in order to optimize the processors' utilization of the cache memory. For example, each of the eight processors may have their own unique partition of the cache if needed to optimize allocation – paragraph 0019, all lines. Note the processors are unallocated until a determination is made as to which processors are to be allocated to their respective cache partitions);

determining whether a set in the optimal allocation sets match requirements for a set of partitions selected for the data processing system (cache optimization can be determined based on cache utilization – paragraph 0021, all lines. In other words, if a running hit average of the cache hits a certain value; the partitions can be allocated to processors in order to optimize the system's efficiency. The system checks to see if the parameters are met or matched to make the determination); and

responsive to a match existing, removing processors in the set from the unallocated processors, wherein cache usage by the processors is optimized for the cache level (paragraph 0021, all lines – again the cache will be repartitioned based on the statistics previously calculated for system efficiency. It is also worthy to note that the system is not just limited in resizing the previous partitions, but it is also capable of reallocating the cache partitions based on the

statistical information. This way, the system can assign processors to partitions in order to optimize the system for that cache level – see paragraphs 0026 and 0027, all lines).

Note also with respect to claim 8, Olarig teaches the additional step of selecting the highest cache level that has been unprocessed in the multi-processor system (as per the example discussed in the previously cited sections, Olarig discuss determining the new partition allocation of the cache). In this example, the cache itself is the highest level of memory (i.e. L1). Additionally, Olarig teaches generating a different set of allocations based on match requirements if no match occurs (again the partitioning will occur based on the need of the system as determined by the statistics collected by the system (paragraphs 0019 and 0020, all lines)).

As for claims 4 and 13, Olarig teaches removing the partition for the set of partitions in response to allocating a set to the partition (paragraph 0019, all lines – once allocated, the partition is no longer available to the remaining processors until the reallocation is determined with the statistical information collected by the system).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig as applied to claims 1 and 10 above, and in further view of Arimilli et al., hereinafter Arimilli '605 (US Patent 6,212,605 B1).

As for claim 2-3 and 11-12, though Olarig teaches his system as including multiple cache levels, he fails to teach repeating the steps of claim 1 (and claim 10) for each cache level by moving from the highest cache level, to each successively lower cache level.

Arimilli '605 however teaches a method for controlling eviction of cache blocks to override the eviction of a value, which is reserved for a later operation. More specifically, Arimilli '605 teaches performing system operations on a hierarchical, multi-level cache (i.e. setting an address reservation flag), by starting at the highest cache level (in this case, L2), and then repeating the system operation on the next lower level - col. 3, lines 46-65.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('605) system of eviction override into his own system of cache partitioning, in order to facilitate repeating the partitioning/allocation techniques of his memory system on each successive level of cache. By doing so, Olarig would benefit by having a means of improving the overall processor performance of his system by avoiding unnecessary evictions to the cache. This way the overall performance will improve, by avoiding a scenario in which a block that has be unnecessarily evicted must be reloaded into the cache as taught by Arimilli '605 – col. 7, lines 38-58.

10. Claims 5-7 and 14-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig as applied to claims 1 and 10 above, and in further view of Arimilli et al., hereinafter Arimilli '115 (US Patent 6,581,115 B1).

As for claims 5-6 and 14-15, though Olarig fails to teach his system as a symmetric multi-processor system (SMP) including L3 and L2 cache, Arimilli '115 teaches a processing system with configurable memory bus and scalability port which specifically apply to an SMP (see abstract), that includes both L2 and L3 cache (col. 5, lines 46-55 and col. 6, lines 19-34).

As for claims 7 and 16, Olarig fails to teach the processors as being located on multi-chip modules, wherein optimal allocations are based on the location of the processors on the modules.

Arimilli '115 however teaches a system containing SMPs, which are located on multi-chip modules (col. 2, lines 20-42). Arimilli '115 further teaches allocating and connecting the processors on the modules to the cache based on bandwidth utilization. In other words, smaller number of processors can be allocated to particular memory partition if the bandwidth allocation needs to be lower. This way, the memory usage can be optimized based on the location of the modules (i.e. more processors located on a bus that has higher allocation, and less processors located on buses with lower bandwidth allocation) –col. 6, lines 19-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('115) data processing system to his own system of cache partitioning. By doing so, Olarig would be able to dynamically

configure a bus allocation of a processor chip utilizing hardware and software allocation methods, and efficiently allocate processor chip bus bandwidth in order to improve the overall data processing system as taught by Arimilli '115 (col. 3, lines 44-56).

11. Claims 9, 17 and 20 rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig, and in further view of Mock et al., hereinafter Mock (US PG Publication 2003/0084372 A1).

As for claims 9 and 17, Olarig fails to teach a memory for storing instructions, which the processors use to carry out the remaining steps of the claim (the remaining steps are discussed under the rejection of claim 1 presented *supra*). Mock however teaches an apparatus for data recovery optimization in a logically partitioned computer system, in which the processors in the multiprocessor system use instructions stored in main memory to carry out their respective functions (paragraph 0034, all lines 1-11).

As for claim 20, Olarig teaches removing the partition for the set of partitions in response to allocating a set to the partition (paragraph 0019, all lines – once allocated the partition is no longer available to the remaining processors until the reallocation is determined with the statistical information collected by the system).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Mock's apparatus for data recovery in a logically partitioned computer system. By doing so, Olarig would benefit by not only having a means of recovering data in his system, but have a system that is capable of implementing a recovery strategy that accurately reflects the current system

configuration. This would in turn increase overall system performance, as discussed by Mock in paragraph 0014, all lines.

12. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaches of Olarig and Mock as applied to claim 17 above, and in further view of Arimilli '605.

As for claim 18-19, though Olarig teaches his system as including multiple cache levels, he fails to teach repeating the steps of claim 1 for each cache level by moving from the highest cache level, to each successively lower cache level.

Arimilli '605 however teaches a method for controlling eviction of cache blocks to override the eviction of a value, which is reserved for a later operation. More specifically, Arimilli '605 teaches performing system operations on a hierarchical, multi-level cache (i.e. setting an address reservation flag), by starting at the highest cache level (in this case, L2), and then repeating the system operation on the next lower level - col. 3, lines 46-65.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('605) system of eviction override into his own system of cache partitioning, in order to facilitate repeating the partitioning/allocation techniques of his memory system on each successive level of cache. By doing so, Olarig would benefit by having a means of improving the overall processor performance of his system by avoiding unnecessary evictions to the cache. This way the overall performance will improve by avoiding a scenario in which it is

necessary to reload a block that been unnecessarily evicted from the cache memory as taught by Arimilli '605 – col. 7, lines 38-58.

13. Claims 21-23 rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teaches of Olarig and Mock as applied to claim 17 above, and in further view of Arimilli '115.

As for claims 21-22, though Olarig fails to teach his system as a symmetric multi-processor system (SMP) including L3 and L2 cache, Arimilli '115 teaches a processing system with configurable memory bus and scalability port which specifically applies to an SMP (see abstract), that includes both L2 and L3 cache (col. 5, lines 46-55 and col. 6, lines 19-34).

As for claim 23, Olarig fails to teach the processors as being located on multi-chip modules, wherein optimal allocations are based on the location of the processors on the modules.

Arimilli '115 however teaches a system containing SMPs, which are located on multi-chip modules (col. 2, lines 20-42). Arimilli '115 further teaches allocating and connecting the processors on the modules to the cache based on bandwidth utilization. In other words, smaller number of processors can be allocated to particular memory if the bandwidth allocation needs to be lower. This was, the memory usage can be optimized based on the location of the modules (i.e. more processors located on a bus that has higher allocation, and less processors located on buses with lower bandwidth allocation) –col. 6, lines 19-35.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Olarig to further include Arimilli's ('115) data processing system to his own system of cache partitioning. By doing so, Olarig would be able to dynamically configure a bus allocation of a processor chip utilizing hardware and software allocation methods, and efficiently allocate processor chip bus bandwidth in order to improve the overall data processing system as taught by Arimilli '115 (col. 3, lines 44-56).

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Franke et al. (US Patent 6,480,941 B1) teach secure partitioning of a shared memory based multiprocessor system.

Brutman et al. (US PG Publication 2003/0101319 A1) teach a method and system for improving cache performance in a multiprocessor computer.

Soltis, JR. (US PG Publication 2003/0172234 A1) teaches a method and system for cache partitioning on large-scale multithreaded, multiprocessor integrated circuits.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

3/14/06
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SUPERVISORY PATENT EXAMINER